Integrated Power Amplifier for 60 GHz Wireless Applications

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Abstract — **This paper presents an integrated power amplifier for the 60 GHz frequency range. The amplifier was fabricated with a commercially available 0.15 µm gate length pseudomorphic HEMT-process. The output stage consists of two 6x35 µm PHEMTs, forming a total output periphery of 420 µm. The MMIC amplifier was simulated, fabricated and measured both on-wafer and in a split block package. The amplifier was characterized using linear and nonlinear methods. The odd mode stability was carefully analyzed. Large-signal scattering parameters were measured with on-wafer probes. The measured gain was 13.4 dB and 1 dB output compression point was at +17 dBm power level using 3.0 V supply voltage. The AM/AM and AM/PM characteristics were extracted from the large-signal S-parameter results. Finally, the amplifier chip was mounted in a split block package, which has WR-15 wave guide input and output interface. The measured results show 12.5 dB small-signal gain and better than 8 dB return losses in input and output for the packaged amplifier chip.**

I. Introduction

The possibilities of the 60 GHz frequency band are interesting, because large bandwidth has been allocated worldwide for wireless networks. Wide bandwidth allows higher data rates to be used and it is more easily available at millimeter wave frequencies. The available frequency bands for 60 GHz broadband networks are gathered in Table I. In Europe the 62–63 GHz and 65–66 GHz bands are allocated for mobile broadband systems (MBS) and the 59–62 GHz band for wireless local area network applications (WLAN). In the United States the 59–64 GHz band is intended for general unlicensed applications. In Japan 59–66 GHz band is reserved for high speed data communication. Thus, 5 GHz of spectral space has been assigned for multimedia services around 60 GHz with a worldwide overlap of 3 GHz (59–62 GHz) [1][2].

The oxygen absorption at 60 GHz range is about 15 dB/km in addition to free space loss, but in office-like environments the more important fact is that, for example, 15 cm thick concrete wall introduces a 36 dB attenuation around 60 GHz. This provides good isolation from nearby transmitters. This frequency range is particularly suitable for indoor short-range communications [1].

In this paper we present an integrated power amplifier for 60 GHz wireless applications. The power amplifier is fabricated using a commercially available 0.15 µm GaAs pseudomorphic HEMT technology. The amplifier is designed using passive and active models provided by the foundry. Both the small-signal and the large-signal models of the transistor were used in the design process.

TABLE I
AVAILABLE FREQUENCY BANDS FOR 60 GHZ WIRELESS BROADBAND NETWORKS [1][2]

Country / Continent	Frequency band [GHz]	Purpose of use
Europe	62–63, 65–66	MBS
	59–62	WLAN
United States	59–64	general
Japan	59–66	data comm.

II. Power Amplifier Design

Our previously fabricated power amplifier design showed that 14 dBm output compression point with 15.5 dB overall gain can be achieved using single transistor output stage. This earlier design, which was presented in [3], is a three stage cascade amplifier with output periphery of 6x35 µm. The gain of the amplifier was optimized by choosing the device peripheries of the driver and the gain stages to be 4x35 µm and 2x35 µm respectively.

In order to achieve higher output power the size of the output stage of the new power amplifier has to be increased. However, larger device periphery of a single transistor leads to a lower gain. This means that the size of the driver and the gain stages have to be increased in order to insure that these stages can drive the output stage into saturation. This might lead to low overall gain of the amplifier. To achieve higher output power level without degrading the gain of the output stage the large transistor can be divided into smaller devices. The power amplifier presented here is a three stage single ended amplifier with total output periphery of 420 µm. The output stage consists of two 6x35 µm cells. In this design the driver and the gain stages were designed to run with 2 dB

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back-off. This was accomplished by choosing both the driver and the gain stages to have device peripheries of 6x35 μm and presenting a proper match to each amplifier stage. The output stage is matched for maximum power whereas the driver stage output match is balanced between optimum power and gain. The gain stage is designed for maximum gain.

Matching at 60 GHz is done with open shunt stubs and series transmission lines as can be seen in the schematic presented in Fig. 1. The matching circuitry of the output stage performs both power combining and dividing as well as the matching of the output cells.

The amplifier is biased through high impedance quarter wave length shunt stubs which are short circuited through a 0.12 pF metal-insulator-metal (MIM) capacitor and a ground via hole. A small valued series resistor (30...50 Ω) at the end of the gate biasing stub is used for out-of-band stabilization. Low frequency stability is insured with 40 Ω resistors that are in series with stabilizing capacitors (5...8 pF). In addition, gate bias is fed through a 100 Ω series resistor.

To suppress any possible odd mode oscillations 80 Ω resistors were added between the output cells [4]. To further enhance the odd mode stability the layout of the output stage was designed to be symmetrical [5]. The odd mode stability of the amplifier was analyzed using the CAD-suitable method described in [6]. The simulated open loop transfer functions of the power amplifier are shown in Fig. 2. The amplifier is stable if $Gi(j\omega)$ (i = 1,2,3 or 4) does not enclose the point 1 + 0j clockwise.

The photograph of the manufactured power amplifier is presented in Fig. 3. Finally, after on-wafer measurements the power amplifier chip was assembled in a split block package. The package has WR-15 wave guide input and output with alumina microstrip transitions. The biasing circuit of the package includes additional RC-networks to improve the low frequency stability. The photograph of the split block package is presented in Fig. 4.

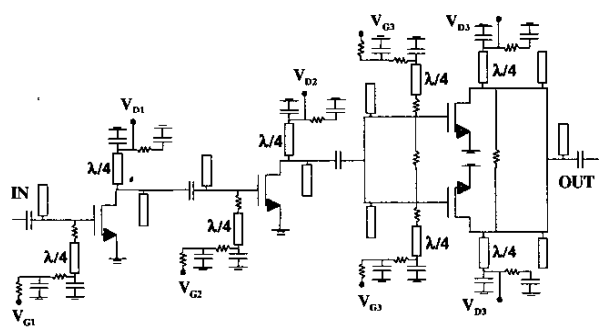

Fig. 1. The schematic of the power amplifier.

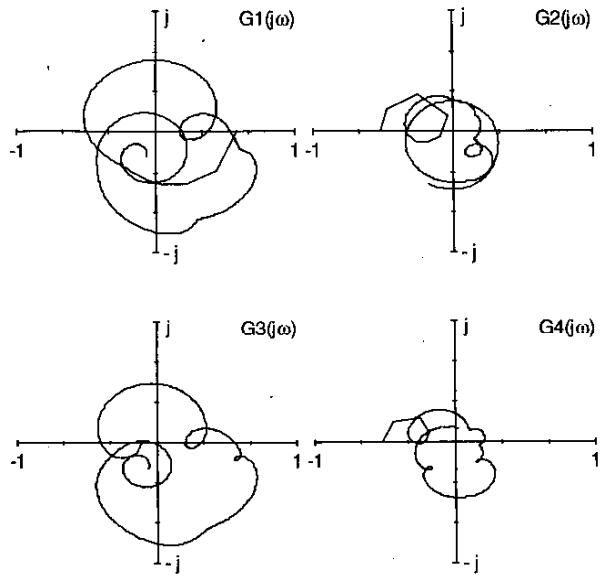

Fig. 2. The simulated (1–120 GHz) Nyquist plots of open-loop transfer functions for the power amplifier.

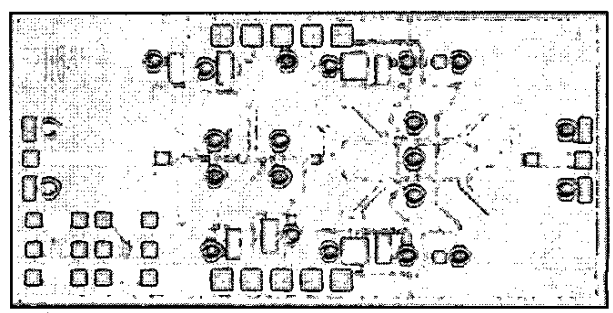

Fig. 3. The photograph of the power amplifier. The chip size is 3 mm x 1.5 mm.

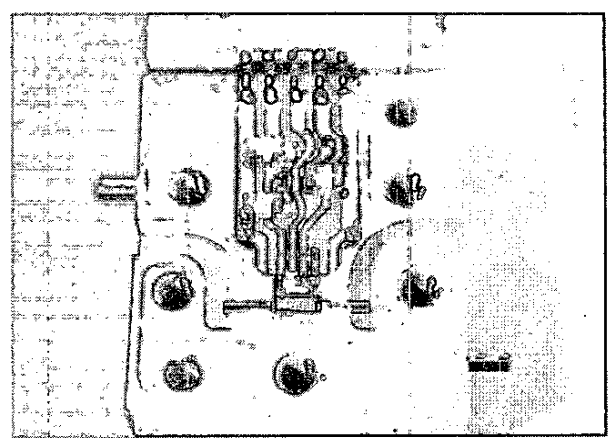

Fig. 4. Photograph of the split block package.

III. Measurement Results

A. On-wafer Measurements

The on-wafer small-signal and large-signal S-parameters were measured with coplanar RF-probes. The measured small-signal S-parameters and equivalent simulated small-signal gain are presented in Fig. 5. The amplifier was biased to nominal 3.0 V of drain voltage and 325 mA of total drain current. The drain currents are 162 mA, 81 mA and 82 mA for the power, driver and the gain stages respectively. Small-signal gain of 13.5 dB is achieved at 62 GHz. The corresponding input and output return losses are around 6.5 dB. As can be seen very good agreement between simulated and measured small signal gain is achieved.

The AM/AM and AM/PM characteristics were extracted from the on-wafer large-signal S-parameter measurements. Because of the high output power level obtained from the measurement system, it was possible to drive the power amplifier into 2 dB compression during the large signal S-parameter measurements, although the amplifier seems to be capable of delivering even more power when driven into deeper saturation. The measured amplitude and phase conversion at 60 GHz frequency are presented in Fig. 6. The simulated output power of the power amplifier is also shown. The amplifier was biased as above. The measured output compression point is at +17 dBm power level and the large signal gain 13.4 dB.

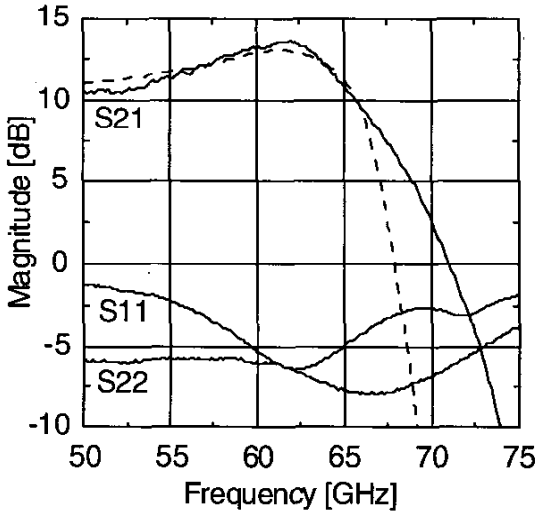

Fig. 5. Measured on-wafer small-signal S-parameters. The dashed line represents simulated S_{21} (Supply voltage / total current: 3.0 V / 325 mA).

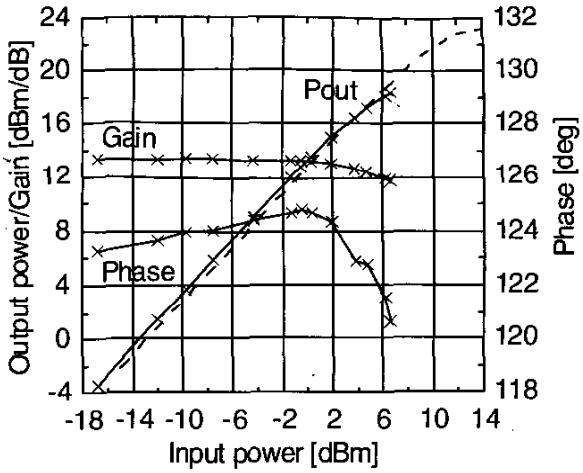

Fig. 6. Measured on-wafer AM/AM and AM/PM characteristics. The dashed line represents the simulated output power (Supply voltage/total current: 3.0 V / 325 mA).

Table II lists the power amplifier large signal characteristics with different supply voltages at 60 GHz. When compared to the previous work, 3 dB higher 1 dB output compression point was achieved.

TABLE II
MEASURED ON-WAFER LARGE-SIGNAL CHARACTERISTICS OF THE POWER AMPLIFIER AT 60 GHZ

Vdd [V]	Ids [mA]	Gain [dB]	Compression point [dBm]
This work			
2.5	324	14	16
3.0	**325**	**13.4**	**17**
3.5	325	12.4	17
4.0	327	11.8	16
Previous work			
3.0	150	15.5	14

B. Module Measurements

The packaged power amplifier was measured in WR-15 wave guide environment. The measured small-signal S-parameters and large signal characteristics of the packaged amplifier are shown in Fig. 7 and Fig. 8 respectively. The small-signal gain is around 12.5 dB. The packaged power amplifier exhibited approximately 1 dB lower small-signal gain when compared to the on-wafer measurements. The input and output return losses of the packaged power amplifier are better than 8 dB at 60 GHz.

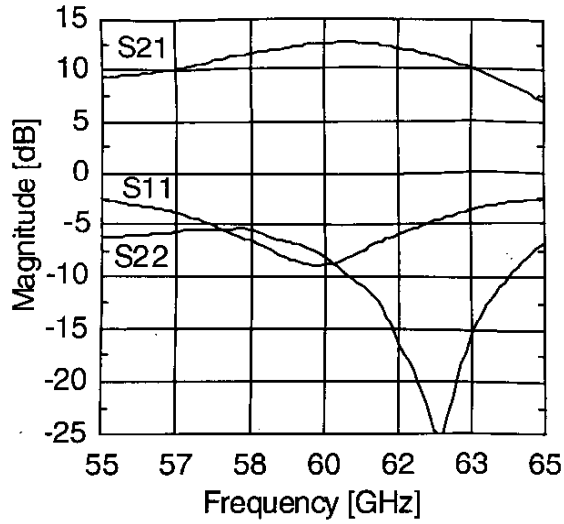

Fig. 7. Measured small-signal S-parameters of the packaged power amplifier (Supply voltage/total current: 3.0 V / 320 mA).

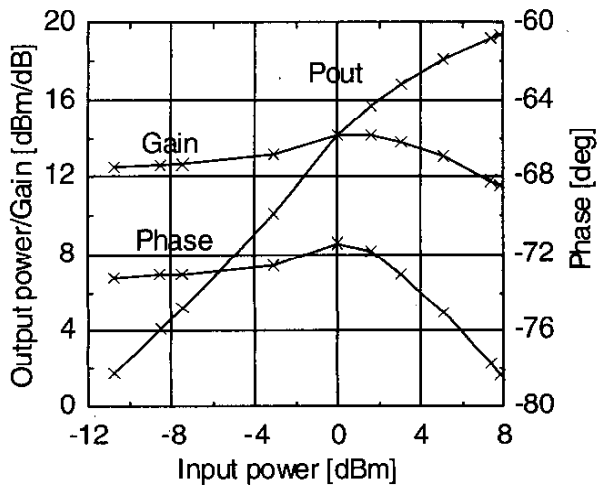

Fig. 8. Measured AM/AM and AM/PM characteristics of the packaged power amplifier (Supply voltage/total current: 3.0 V / 320 mA).

IV. Conclusion

We presented a 60 GHz integrated power amplifier, which was simulated, fabricated, packaged and measured. Extensive precaution was practiced to make sure that the amplifier is stable in both cases of oscillation modes of a multidevice amplifier. The AM/AM and AM/PM conversion of the power amplifier was presented. Large-signal scattering parameters were measured both on-wafer and in a split block package.

Acknowledgement

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